IN THE CLAIMS

Please cancel Claims 23-32 without prejudice or disclaimer.

Please add the following new Claims:

New Claim 33. A semiconductor package comprising:

a substrate on which a plurality of circuit patterns is formed;

a first semiconductor chip having first and second surfaces wherein the first surface of the first semiconductor chip is coupled to the substrate,

a plurality of input-output pads formed on the second surface of the first semiconductor chip;

an adhesive layer coupled to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces;

means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the means coupled to the first surface thereof;

a plurality of input-output pads formed on the second surface thereof;

a plurality of first conductive wires connecting the input-output pads of the first semiconductor chip and the circuit pattern of the substrate;

a plurality of second conductive wires connecting the input-output pads of the second semiconductor chip and the circuit pattern of the substrate; and

means for sealing the first semiconductor chip, the adhesive layer, the second semiconductor chip, insulator, and the first and the second conductive wires.

New Claim 34. A semiconductor package in accordance with Claim 33 wherein the substrate is one selected from a group consisting of a printed circuit board, a circuit tape, a circuit film, a lead frame, and combinations thereof.

New Claim 35. A semiconductor package in accordance with Claim 33 further comprising a conductive ball coupled to a surface of the substrate.

New Claim 36. A semiconductor package in accordance with Claim 33 wherein the substrate has a perforating hole of which size is larger than that of the first semiconductor chip.

New Claim 37. A semiconductor package in accordance with Claim 33 wherein the means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds is an insulator.

New Claim 38. A semiconductor package in accordance with Claim 33 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

New Claim 39. A semiconductor package comprising:

a substrate;

a first semiconductor chip coupled to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

a second semiconductor chip having first and second surfaces which are substantially flat in nature;

means coupled to the second surface of the first semiconductor chip for adhering the first semiconductor chip to the second semiconductor chip;

means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof;

at least one input-output pad being formed on the second surface of the first semiconductor chip; and

at least one first conductive wire connecting the input-output pad of the first semiconductor chip and the substrate.

at least one input-output pads formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the input-output pads of the second semiconductor chip and the substrate.

New Claim 40. A semiconductor package in accordance with Claim 39 wherein the means coupled to the second surface of the first semiconductor chip is an adhesive layer.

New Claim 41. A semiconductor package in accordance with Claim 40 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

New Claim 42. A semiconductor package in accordance with Claim 39 wherein the means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

CLEAN VERSION OF NEW CLAIMS

Claim 33. A semiconductor package comprising:

a substrate on which a plurality of circuit patterns is formed;

a first semiconductor chip having first and second surfaces wherein the first surface of the first semiconductor chip is coupled to the substrate,

a plurality of input-output pads formed on the second surface of the first semiconductor chip;

an adhesive layer coupled to the second surface of the first semiconductor chip;

a second semiconductor chip having first and second surfaces;

means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the means coupled to the first surface thereof;

a plurality of input-output pads formed on the second surface thereof;

a plurality of first conductive wires connecting the input-output pads of the first semiconductor chip and the circuit pattern of the substrate;

a plurality of second conductive wires connecting the input-output pads of the second semiconductor chip and the circuit pattern of the substrate; and

means for sealing the first semiconductor chip, the adhesive layer, the second semiconductor chip, insulator, and the first and the second conductive wires.

Claim 34. A semiconductor package in accordance with Claim 33 wherein the substrate is one selected from a group consisting of a printed circuit board, a circuit tape, a circuit film, a lead frame, and combinations thereof.

Claim 35. A semiconductor package in accordance with Claim 33 further comprising a conductive ball coupled to a surface of the substrate.

Claim 36. A semiconductor package in accordance with Claim 33 wherein the substrate has a perforating hole of which size is larger than that of the first semiconductor chip.

Claim 37. A semiconductor package in accordance with Claim 33 wherein the means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds is an insulator.

Claim 38. A semiconductor package in accordance with Claim 33 wherein the insulator is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.

Claim 39. A semiconductor package comprising:

a substrate;

a first semiconductor chip coupled to a surface of the substrate, the first semiconductor chip having first and second surfaces which are substantially flat in nature;

a second semiconductor chip having first and second surfaces which are substantially flat in nature;

means coupled to the second surface of the first semiconductor chip for adhering the first semiconductor chip to the second semiconductor chip;

means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds wherein the second semiconductor chip is coupled to the adhesive layer by the insulator coupled to the first surface thereof;

at least one input-output pad being formed on the second surface of the first semiconductor chip; and

at least one first conductive wire connecting the input-output pad of the first semiconductor chip and the substrate.

at least one input-output pads formed on the second surface of the second semiconductor chip; and

at least one second conductive wire connecting the input-output pads of the second semiconductor chip and the substrate.

Claim 40. A semiconductor package in accordance with Claim 39 wherein the means coupled to the second surface of the first semiconductor chip is an adhesive layer.

Claim 41. A semiconductor package in accordance with Claim 40 wherein the adhesive layer is one selected from a group consisting of: nonconductive liquid phase adhesive, a nonconductive adhesive tape, and combinations thereof.

Claim 42. A semiconductor package in accordance with Claim 39 wherein the means coupled to the first surface of the second semiconductor chip for preventing shorting of wirebonds is one selected from a group consisting of: a nonconductive liquid phase adhesive, a nonconductive adhesive tape/film, a polyimide, an oxide layer, a nitride layer, and combinations thereof.